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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,610	06/26/2003	Frank C. Wirtz II	X-1125 US	4919

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EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,610	WIRTZ ET AL.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *52* is/are allowed.

6)☒ Claim(s) *1,2,6,7,15,20,24,26,36-38 and 43-48* is/are rejected.

7)☒ Claim(s) *3-5,8-14,16-18,21-23,25,27-35,39-42 and 49-51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6-23-2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 15, 26, 38 and 45-46 are rejected under 35 U.S.C. 102(b) as being anticipated by Ong et al. (US PAT No. 5,821,772).

Regarding claim 1, Fig. 2 of Ong et al. teaches an integrated circuit comprising: a configurable function unit (21, Counter is designed, i.e. configured not to provide the count 00000; col. 3, lines 6-10) including a configurable function unit component (a counter is inherently comprised of configurable function units, e.g. logic gates); and at least one configurable decoder (DEC0 - DEC15 are programmed or configured by BITSTREAM1) having decoder configuration data (data in A0-1 - A0-5 in DEC0) and a decoder output (output of AND00), the configurable decoder being operable to decode a value in data presented by the configurable function unit component (output data presented by counter 21); wherein the configurable decoder is optimized to assert the decoder output based on a comparison of the decoder configuration data with the value presented by the configurable function unit component (decoder 21 is optimized to provide loading the data in different order; col. 3, lines 25-37).

Regarding claim 2, Fig. 2 of Ong et al. teaches the integrated circuit of claim 1, wherein the decoder configuration data is specified by configuring decoder cells having cell values of binary logic one, and binary logic zero, (address memory cells A0-1 - A0-5 are filled with binary logic one and/or zero respectively) and wherein the decoder output is asserted when the value presented by the configurable function unit component are consistent with the cell values (XNOR gates X0-1 - X0-5 perform comparison and provides output when data are matched, i.e. consistent with counter output).

Regarding claim 15, Fig. 2 of Ong et al. teaches the integrated circuit of claim 1, where the configurable function unit component is a counter (21 is counter).

Regarding claim 19, Fig. 2 of Ong et al. teaches the integrated circuit of claim 15 where the decoder output is synchronized and provided to the logical interconnect network (when the counter 21 provides the count that is the same as the address memory cells A0-5 through A0-1, AND gate AND00 provides high signal to the address line A0, i.e. the output of the decoder is synchronized).

Regarding claim 26, Fig. 2 of Ong et al. teaches a programmable logic device comprising: a counter (21) providing a counter value (MSB - LSB); a decoder (DEC0 - DEC5) configurable to provide an output signal (output of AND00) in response to a selected counter value (data in A0-1 -A-5); and an

interconnect matrix (lines in 20) for interconnecting the programmable logic, and receiving the output signal (output of AND00 - AND05 is connected to respective lines).

Regarding claim 38, Fig. 2 of Ong et al. teaches a programmable logic device (FPGA) comprising programmable logic (FPGA has logic blocks and routing configured by memory cells; col. 1, lines 15-20); a shift register (address memory cells A0-5 through A0-1; col. 3, lines 11-14) providing a shift register value (the count 00001; col. 3, line 15); a decoder (DEC0 - DEC15) configurable to provide an output signal (output of AND00 - AND 15) in response to a selected shift register value (data in A0-1 - A15-5 are compared with counter 21 output); and an interconnect matrix (conductor lines in 20) for interconnecting the programmable logic, and receiving the output signal (logic blocks receives the output of AND00 - AND15).

Regarding claim 45, Fig. 2 of Ong et al. teaches a CPLD having interconnectable programmable logic (FPGA has logic blocks configured by memory cells; col. 1, lines 15-20), configuration memory (M0-0 - M15-15), and external inputs and outputs (external inputs and outputs are inherent in a FPGA to communicate with other devices), the interconnectable programmable logic being connected by a logical interconnection matrix (FPGA has routing configured by memory cells; col. 1, lines 15-20), and the CPLD comprising: a configurable function unit (21, Counter is designed, i.e. configured not to provide

the count 00000; col. 3, lines 6-10) including a configurable function unit component (a counter is inherently comprised of configurable function units, e.g. logic gates); and a configurable decoder (DEC0 - DEC15 are programmed or configured by BITSTREAM1) operable to assert a decoder output upon detecting a decode value in data presented by the configurable function unit component (decoder 21 is optimized to provide loading the data in different order; col. 3, lines 25-37).

Regarding claim 46, Fig. 2 of Ong et al. teaches the CPLD of claim 45, wherein a decoder configuration associated with the configurable decoder comprises decoder cells, which are configured to match output bits of the configurable function unit component corresponding to binary logic one, binary logic zero, (address memory cells A0-1 - A0-5 are filled with binary logic one and/or zero respectively) and corresponding to a value that matches either binary logic one, binary logic zero, or that matches both binary logic one and binary logic zero (XNOR gates X0-1 - X0-5 perform comparison and provides output when data are matched, i.e. consistent with counter output).

Regarding claim 47, Fig. 2 of Ong et al. teaches the CPLD of claim 45 where the configurable function unit is logically internal to a predetermined function block of the CPLD (the counter 21 is within a decoder structure (predetermined function) having a programmable address decoder with a counter).

Regarding claim 48, Fig. 2 of Ong et al. teaches the CPLD of claim 45 where the configurable function unit is logically internal to a predetermined specialized macrocell logically within the predetermined function block (the counter 21 is within a decoder structure (predetermined specialized macrocell) having a programmable address decoder with a counter).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-7, 36-37 and 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ong et al. in view of New (US PAT No. 6,288,570).

Regarding claims 6, 36 and 43, Fig. 2 of Ong et al. teaches the integrated circuit of claims 1, 26 and 38 as discussed above where the FPGA includes logic blocks, but does not teach the integrated circuit is an FPGA including at least one look-up table. However, Fig. 12a of New discloses a configurable logic blocks including at least one look-up table (J, H, G, F) for the purpose of providing simple implementation of any one of logic functions (col. 7, lines 25-26, col. 13, lines 55-56). Therefore, it would have been at the time the invention was made to a person ordinary skilled in art to implement the look-up table of New in the logic block of Ong et al. to simplify implementation of a logic function.

Regarding claims 7, 37 and 44, Fig. 2 of Ong et al. teaches the integrated circuit of claims 1, 26 and 38 as discussed above where the FPGA is a complex programmable logic device (FPGA is complex device compared to a logic gate) including logic blocks, but does not teach the logic blocks including a plurality of macrocells. However, Fig. 12a of New discloses a configurable logic blocks including look-up tables (each look-up table, J, H, G, F performs a macrofunction, i.e. a macrocell) for the purpose of providing simple implementation of any one of logic functions (col. 7, lines 25-26, col. 13, lines 55-56). Therefore, it would have been at the time the invention was made to a person ordinary skilled in art to implement the look-up tables of New in the logic block of Ong et al. to simplify implementation of a logic function.

Claims 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ong et al. in view of Higashitsutsumi (US PAT No. 5,226,063).

Regarding claims 20 and 24, Fig. 2 of Ong et al. teaches the integrated circuit of claim 1 where the configurable function unit component is a counter designed not provide the count 0000 (col. 3, lines 6-10), but does not disclose the counter is a shift register or a feedback shift register. However, Fig. 5 of Higashitsutsumi teaches a counter comprising of shift registers (15a, 15b, 15c, 15d) with a feedback from the output of 15d and 15a to the input of 15a via an exclusive NOR gate for the purpose of providing a polynominal function. Therefore it would have been obvious at the time the invention was made to a

person ordinary skill in the art to utilize the polynominal counter having shift registers with feedback of Higashisutsumi in place of the counter of Ong et al. since it would provide a polynominal function.

Allowable Subject Matter

Claim 52 is allowable over the prior art of record.

Claims 3-5, 8-14, 16-18, 21-23, 25, 27-35, 39-42 and 49-51 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although Ong et al. teaches a FPGA with programmable address decoder, New teaches a programmable logic device with a configuration logic blocks and Higashitsutsumi teaches a polynominal counter, one of ordinary skill in the art would not have been motivated to modify the teaching of Ong et al. and/or New and/or Higashitsutsumi to further includes, among other things, the specific of the decoder cells have cell values of "don't care" as recited in claims 3, 27, 39, a cascade output of the configurable decoder is provided to the second configurable function unit to facilitate combining the first configurable function unit with the second configurable function unit as recited in claim 4, 40, the configurable function unit is associated with a predetermined function block of the function blocks of the CPLD as recited in claim 8, an input of the configurable function unit comprising a configurable product term as recited in claim 14, the configurable decoder is operable to match a predetermined value one clock cycle

before the configurable function unit component reaches the predetermined value as recited in claim 16, the configurable decoder is operable to match a specified terminal value and, based on reaching the specified terminal value, to cause a reset of the configurable function unit component as recited in claim 17, 31, the configurable decoder is operable to match a predetermined value within the shift register one clock cycle before the shift register contains a particular shift register value as recited in claim 21, the configurable function unit component being a cyclic redundancy check generator, a serial encrypter or an accumulator as recited in claims 22, 23 and 25 , a cascade output of the decoder is provided to the programmable logic device to facilitate combining the counter with at least one other counter in the programmable logic device as recited claim 28, the decoder output is synchronized by and provided to the rest of the CPLD through a macrocell register associated with the predetermined specialized macrocell as recited in claim 49, the decoder output is provided via a value rail to at least one macrocell in the predetermined function block other than the predetermined specialized macrocell recited in claim 50, the decoder output is synchronized by and provided to the rest of the CPLD through a macrocell register in a macrocell other than the predetermined specialized macrocell recited in claim 51, a configurable function unit including a function unit component and at least one configurable decoder programmable to decode a particular value as stored in the configuration memory when the particular value is presented by the function unit component, and the logical function unit inputs

performing substantially the same functions as macrocell control inputs associated with the conventional macrocells as recited in claim 52.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Inuzuka et al. (US PAT No. 5,777,946) discloses a column addressing circuit having a shift register.

Trimberger (US PAT No. 5,426,379) discloses an FPGA with built-in bitstream data expansion.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

Date: 12-1-2004